

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,447,290 B2
APPLICATION NO. : 10/709026
DATED : November 4, 2008
INVENTOR(S) : Yuan-Kun Hsiao

Page 1 of 3

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

The title page showing the illustrative figure should be deleted to be replaced with the attached title page.

The drawing sheet, consisting of Fig. 2, should be deleted to be replaced with the drawing sheet, consisting of Fig. 2, as shown on the attached page.

In the Drawings:

On Sheet 2 of 3, in FIG. 2, Box 42, line 1, delete "Filp-flop" and insert -- Flip-flop --, therefor.

On Sheet 2 of 3, in FIG. 2, Box 44, line 1, delete "Filp-flop" and insert -- Flip-flop --, therefor.

In column 2, line 43, after "addition," delete "A" and insert -- a --, therefor.

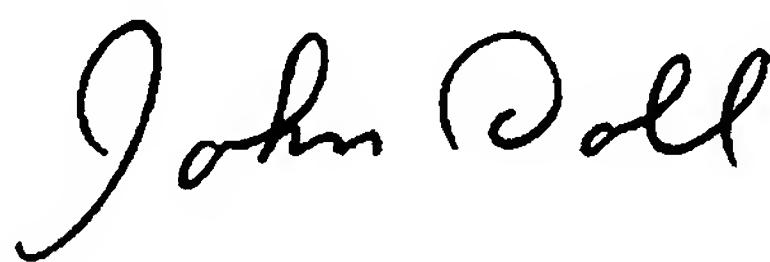
In column 7, line 50, delete "to," and insert -- t0, --, therefor.

In column 8, line 35, delete "t11," and insert -- t15, --, therefor.

In column 9, line 10, delete "PS)" and insert -- P5) --, therefor.

Signed and Sealed this

Tenth Day of March, 2009



JOHN DOLL
Acting Director of the United States Patent and Trademark Office

(12) United States Patent
Hsiao

(10) Patent No.: US 7,447,290 B2
(45) Date of Patent: Nov. 4, 2008

(54) APPARATUS OF PHASE-FREQUENCY
DETECTOR 6,387,417 B2 7/26/03 Okamoto
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6,754,147 B2 6/20/04 Hsu

(75) Inventor: Yuan-Kun Italan, Taipei Hsien (TW)

(73) Assignee: **Tian Holdings, LLC, Wilmington, DE
(US)**

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 830 days.

(21) Appl. No.: 10/709,026

(22) Filed: Apr. 7, 2004

(65) Prior Publication Data
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(S2) U.S. CL 375/375; 375/215; 375/371;
375/376; 327/3; 327/5; 327/7; 327/156; 369/44.13;
369/44.26

(S8) Field of Classification Search 375/326,
375/362, 371, 373, 375-376, 315, 354; 327/113,

See application file for complete search history.

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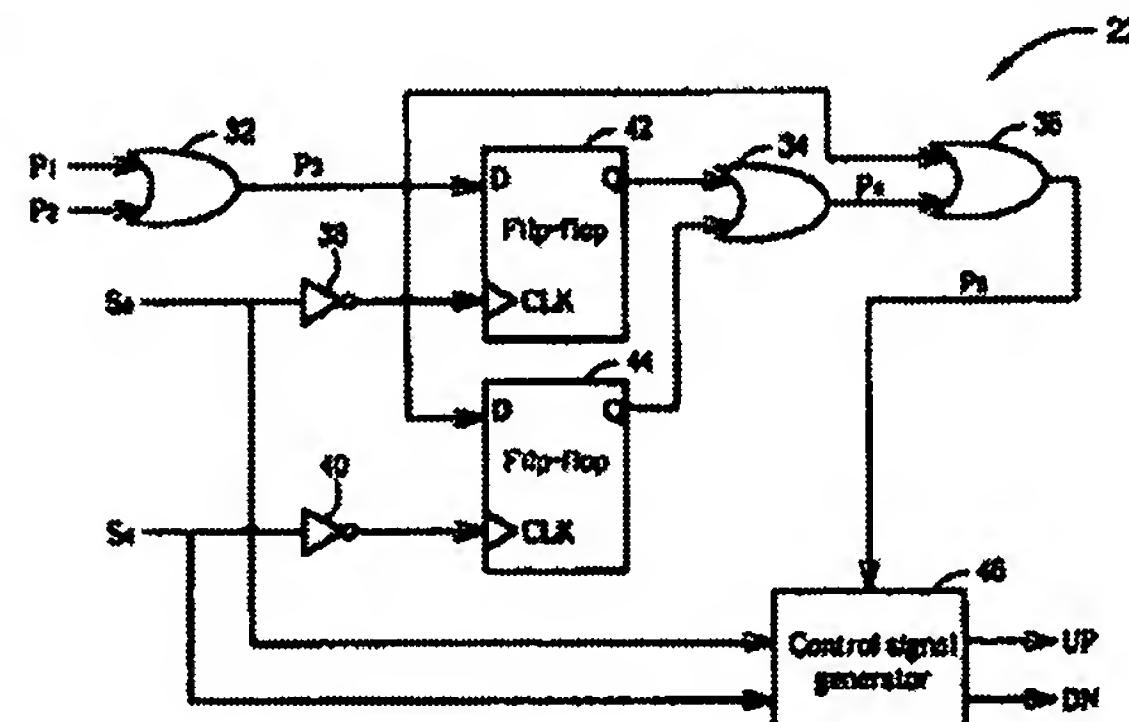
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Primary Examiner—Shuwang Liu
Assistant Examiner—Hirdepal Singh
(74) Attorney, Agent, or Firm—Perkins Coie LLP

(57) ABSTRACT

An apparatus of phase-frequency detector for adjusting wobble clock signal and wobble signal in the same phase, comprising: a first logic gate, receiving a first protection signal and a second protection signal and outputting a third protection signal according to a logic operation; a first flip-flop, coupled to the first logic gate, outputting the third protection signal as a first output signal when the wobble clock trigger; a second flip-flop, coupled to the first logic gate, outputting the third protection signal as a second output signal when the wobble signal trigger; a second logic gate, coupled to the first and the second flip-flop, outputting a fourth protection signal according to a logic operation; a third logic gate, coupled to the second logic gate, receiving the third and the fourth protection signal, and outputting a fifth protection signal according to a logic operation; and a control signal generator, receiving the wobble clock, the input signal, and the fifth protection signal and determining whether adjusting the phase of the wobble signal and the wobble clock according to the logic level of the fifth protection signal.

21 Chats, 3 Drawing Sheets



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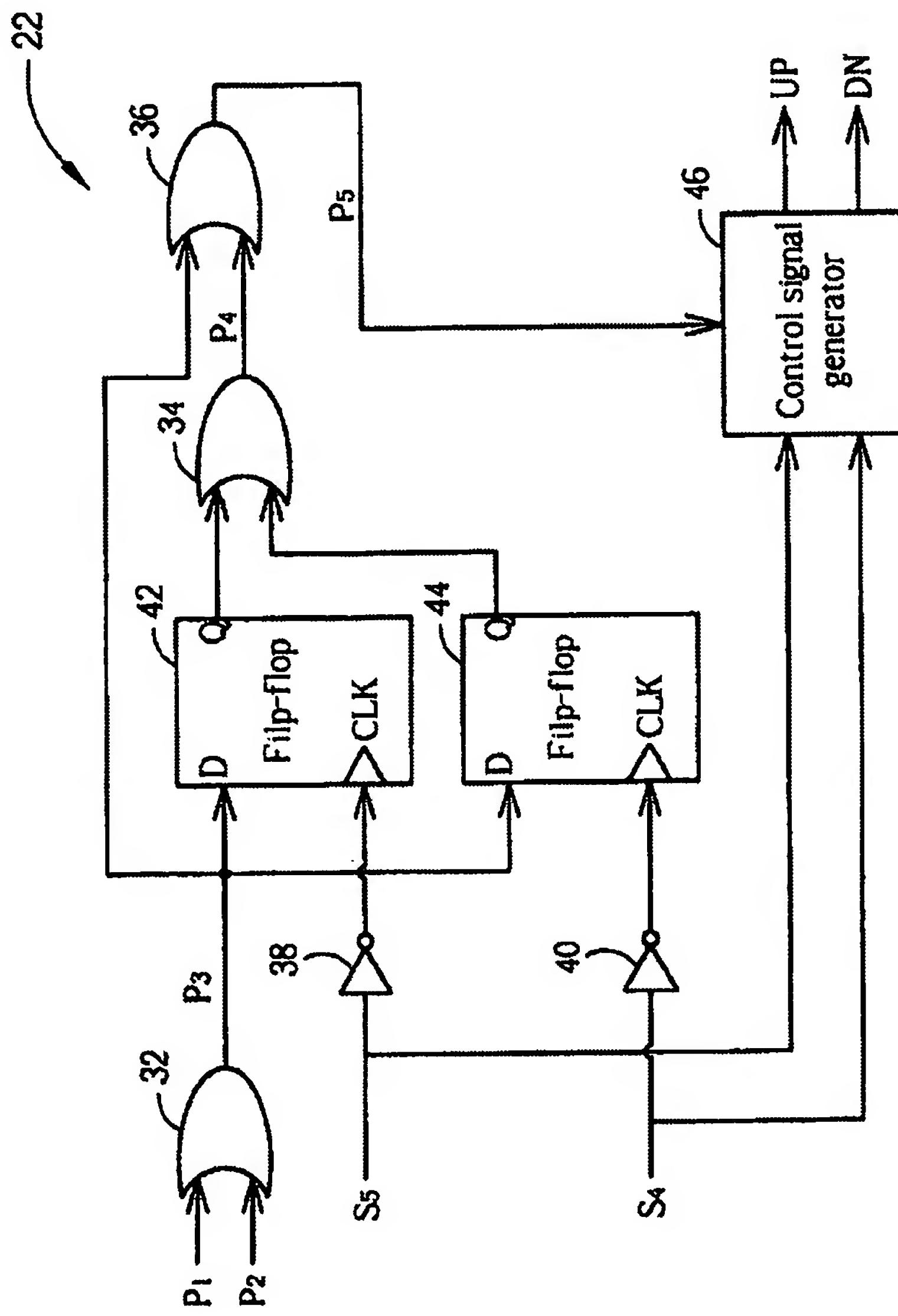


Fig. 2